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10/730,319	12/08/2003	Toshiaki Fukushima	JP920030131US1	2405

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EXAMINER	
BERTRAM, RYAN	

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2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,319	FUKUSHIMA ET AL.	
	Examiner	Art Unit	
	Ryan Bertram	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/3/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

I. OBJECTIONS TO THE SPECIFICATION

Specification

The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code on Page 2 under "Description of Related Art". Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

II. DOUBLE PATENTING

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 7, and 15 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 31 and 36 of copending Application No. 10/73021 in view of Pollard, II et al. (US 7,050,959) hereinafter Pollard.

This is a provisional obviousness-type double patenting rejection.

10/730,319	***10/730,321***
1. A setting device for setting a memory control device which accesses a memory module implementing a memory device therein, comprising: a memory attribute information acquisition unit for acquiring memory attribute information indicating an attribute of the memory module from an attribute memory provided in the memory module;	31. An apparatus, comprising: a memory that includes instructions for: acquiring first memory attribute information for a first memory module from an attribute memory in the first memory module;
and a transfer rate setting unit for determining, based on the memory attribute information, a data transfer rate setting value as a rate of an upper limit value of a data transfer rate relative to a maximum data transfer rate,	Determining a first data transfer rate setting value for the first memory module based at least in part upon the acquired first memory attribute information;
and for setting the determined data transfer rate setting value in the memory control device, the upper limit value of the data transfer rate being at which the memory control device accesses the memory module, and the maximum data transfer rate being at which the memory control device is able to access the memory module.	*Pollard* teaches the upper limit value of the data transfer rate [Col. 3, lines 43-52] and the maximum data transfer rate [see Col. 4, lines 46-49]
7. The setting device according to claim 1, wherein the memory module is attached into any of a plurality of memory slots provided in an information processing apparatus, the setting device further includes a memory attachment position information acquisition unit for acquiring memory attachment position information indicating into which of the memory slots	36. The apparatus of claim 1, wherein the memory comprises additional instructions for: acquiring the first memory attachment position information that is indicative of a memory slot to which the first memory module is attached;

the memory module is attached,	
and the transfer rate setting unit determines the data transfer rate setting value based on the memory attribute information and the memory attachment position information, and sets the determined data transfer rate setting value in the memory control device.	Determining the first data transfer rate setting value based at least in part upon the first memory attribute information and the first memory attachment position information
15. An information processing apparatus, comprising: a memory module implementing a memory device therein; a memory attribute information acquisition unit for acquiring memory attribute information indicating an attribute of the memory module from an attribute memory provided in the memory module; a memory control device for accessing the memory module;	31. An apparatus, comprising: a memory that includes instructions for: acquiring first memory attribute information for a first memory module from an attribute memory in the first memory module;
and a transfer rate setting unit for determining, based on the memory attribute information, a data transfer rate setting value as a rate of an upper limit value of a data transfer rate relative to a maximum data transfer rate, and for setting the determined data transfer rate setting value in the memory control device, the upper limit value of the data transfer rate being at which the memory control device accesses the memory module, and the maximum data transfer rate being at which the memory control device is able to access the memory module.	*Pollard* teaches the upper limit value of the data transfer rate [Col. 3, lines 43-52] and the maximum data transfer rate [see Col. 4, lines 46-49]

The invention of claims 1, 7, and15 differs from the invention of claimed in application 10/730,321 as shown above.

Pollard teaches setting the determined data transfer rate setting value in the memory control device **[see Col. 5, Lines 1-4]**, the upper limit value of the data transfer rate being at which the memory control device accesses the memory module **[see Col. 3, Lines 43-52, "Maximum sustainable power"]**, and the maximum data transfer rate being at which the memory control device is able to access the memory module **[see Col. 4, Lines 46-49, "Maximum threshold bandwidth"]**.

Application 10/730,321 and Pollard are analogous art because they are from the same field of endeavor, managing heat and temperature within memory modules.

At the time of invention, it would have been obvious to modify the system of 10/730,321 with the data transfer rate setting method of Pollard.

The motivation for doing so would have been to allow a system to run at near optimum performance levels without exceeding specified maximum temperature thresholds **[see abstract]**.

Therefore it would have been obvious to combine Pollard with application 10/730,321 for the benefit of maximum system performance to obtain the invention as specified in claims 1, 7, and 15.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Pollard, II et al, (US 7,050,959) hereinafter Pollard.

1. Regarding claim 1, Pollard teaches a setting device for setting a memory control device which accesses a memory module implementing a memory device therein, comprising:

a memory attribute information acquisition unit for acquiring memory attribute information indicating an attribute of the memory module from an attribute memory provided in the memory module **[see Col. 5, Lines 26-36]**;

a transfer rate-setting unit **[see Fig. 1, Element 110, "BIOS"]** for determining, based on the memory attribute information **[see Col. 3, Lines 40-43]**, a data transfer rate setting value as a rate of an upper limit value of a data transfer rate (maximum sustainable power) relative to a maximum data transfer rate **[see Col. 3, Lines 43-52 & Col. 4, Lines 32-45, "Maximum sustainable power represents upper limit value of**

the data transfer"], and for setting the determined data transfer rate setting value in the memory control device **[see Col. 5, Lines 1-4]**, the upper limit value of the data transfer rate being at which the memory control device accesses the memory module **[see Col. 3, Lines 43-52, "Maximum sustainable power"]**, and the maximum data transfer rate being at which the memory control device is able to access the memory module **[see Col. 4, Lines 46-49, "Maximum threshold bandwidth"]**.

2. Regarding claim 2, Pollard teaches the setting device according to claim 1, wherein the transfer rate setting unit determines an upper limit value of a number of memory accesses issued by the memory control device per unit time as the data transfer rate setting value based on the memory attribute information, and sets the determined upper limit value in the memory control device **[see Col. 5, Lines 9-16, "Read/write requests"]**.

3. Regarding claim 3, Pollard teaches the setting device according to claim 1, wherein the transfer rate setting unit determines a value indicating a number of idle cycles while the memory control device is not performing memory accesses as the data transfer rate setting value based on the memory attribute information, each idle cycle being inserted between one cycle while the memory control device is performing a memory access and the other to set the determined value in the memory control device **[see Col. 5, Lines 16-24]**.

4. Regarding claim 4, Pollard teaches the setting device according to claim 1, wherein the memory module generates heat by being accessed by the memory control device **[see Col. 1, Lines 15-21]** and the transfer rate setting unit determines a data transfer rate setting value for maintaining a temperature of the memory module at a predetermined upper limit temperature or lower based on the memory attribute information, and sets the determined data transfer rate setting value in the memory control device **[see Col. 5, Lines 4-9]**.

5. Regarding claim 5, Pollard teaches the setting device according to claim 4, wherein, as setting for maintaining the memory module at the upper limit temperature or lower, the transfer rate setting unit determines, as the data transfer rate setting value, a smaller value in a case where a heating value of the memory module is larger as compared with a value in a case where the heating value of the memory module is smaller, and sets the determined data transfer rate setting in the memory control device **[see Col. 5, Lines 4-9].**

6. Regarding claim 6, Pollard teaches the setting device according to claim 4, further comprising an upper limit temperature acquisition unit for acquiring an upper limit temperature at which the memory module is operated,

wherein the transfer rate setting unit determines a data transfer rate setting value for maintaining the temperature of the memory module at the upper limit temperature or lower based on the memory attribute information, and sets the determined data transfer rate setting value in the memory control device **[see Col. 4, Lines 32-37]**.

7. Regarding claim 7, Pollard teaches the setting device according to claim 1,

wherein the memory module is attached into any of a plurality of memory slots provided in an information processing apparatus **[see Col. 3, Lines 58-60]**;

the setting device further includes a memory attachment position information acquisition unit for acquiring memory attachment position information indicating into which of the memory slots the memory module is attached **[see Col. 3, Line30-40]**;

the transfer rate setting unit determines the data transfer rate setting value based on the memory attribute information and the memory attachment position information, and sets the determined data transfer rate setting value in the memory control device **[see Col. 5, Lines 47-55]**.

8. Regarding claim 8, Pollard teaches the setting device according to claim 1, wherein the setting device is a device for setting the data transfer rates for a plurality of the memory modules **[see Col. 3, Lines 58-60]** attached into an information processing apparatus **[see Fig. 1, Element 110]**,

the memory attribute information acquisition unit acquires the memory attribute information of the plurality of memory modules for each thereof in association therewith **[see Col. 5, Lines 26-36]**,

the transfer rate setting unit creates individual setting values as data transfer rate setting values set when the memory modules are singly attached into the information processing apparatus for each of the plurality of memory modules based on the memory attribute information of the memory modules **[see Col. 3, Line 60 - Col. 4, Line 4]**, and determines a value between maximum and minimum values of the individual setting values, each of which is created so as to correspond to each of the plurality of memory modules, as a data transfer rate setting value for the plurality of memory modules **[see Col. 4, Lines 33-40]**.

9. Regarding claim 9, Pollard teaches the setting device according to claim 1, wherein the setting device is a device for setting the data transfer rates for a plurality of the memory modules **[see Col. 3, Lines 58-60]** attached into an information processing apparatus **[see Fig. 1, Element 110]**,

the memory attribute information acquisition unit acquires the memory attribute information of the plurality of memory modules for each thereof in association therewith **[see Col. 5, Lines 26-36]**,

the transfer rate setting unit creates individual setting values as data transfer rate setting values set when the memory modules are singly attached into the information processing apparatus for each of the plurality of memory modules based on the memory

attribute information of the memory modules **[see Col. 3, Line 60 - Col. 4, Line 4]**, and determines a minimum value of the individual setting values, each of which is created so as to correspond to each of the plurality of memory modules, as a data transfer rate setting value for the plurality of memory modules **[see Col. 5, Lines 46-55]**.

10. Regarding claim 10, Pollard teaches the setting device according to claim 1, wherein the memory attribute information acquisition unit acquires type identification information identifying a type of any of the memory module and the memory device as the memory attribute information **[see Col. 3, Lines 19-30]**, and

the transfer rate setting unit determines the data transfer rate setting value in accordance with the type identification information, and sets the determined data transfer rate setting value in the memory control device **[see Col. 4, Lines 33-40]**.

11. Regarding claim 11, Pollard teaches the setting device according to claim 11,

wherein the transfer rate setting unit determines the data transfer rate setting value in accordance with the manufacturer identification information, and sets the determined data transfer rate setting value in the memory control device **[see Col. 4, Lines 54-67]**.

12. Regarding claim 12, Pollard teaches the setting device according to claim 1,

wherein the memory attribute information acquisition unit acquires number-of-devices information indicating a number of the memory devices implemented in the memory module as the memory attribute information **[see Col. 5, Lines 26-36]**.

13. Regarding claim 13, Pollard teaches the setting device according claim 1,

wherein the memory module includes a board implementing at least one memory device thereon **[see Col. 3, Lines 58-66]**,

the memory attribute information acquisition unit acquires, as the memory module is a memory module of single-sided implementation, which implements the memory device on one side of the board or a memory module of double-sided implementation, which implements the memory devices on both sides of the board **[see Col. 3, Lines 3040,**

the transfer rate setting unit determines the data transfer rate setting value in accordance with the memory bank information, and sets the determined data transfer rate setting value in the memory control device **[see Col. 5, Lines 1-9]**.

14. Regarding claim 14, Pollard teaches the setting device according to claim 13,

wherein the transfer rate setting unit determines, as the data transfer rate setting value, a smaller value in a case where the memory bank information indicates the memory module of the double-sided implementation as compared with a value in a case where the memory bank information indicates the memory module of the single-sided

implementation, and sets the determined data transfer rate setting value in the memory control device **[see Col. 4, Lines 33-40]**.

15. Regarding claim 15, Pollard teaches an information processing apparatus, comprising:

a memory module implementing a memory device therein **[see Fig. 1]**;

a memory attribute information acquisition unit for acquiring memory attribute information indicating an attribute of the memory module from an attribute memory provided in the memory module **[see Col. 5, Lines 26-36]**;

a memory control device for accessing the memory module **[see Fig. 1]**; and

a transfer rate-setting unit **[see Fig. 1, Element 110, "BIOS"]** for determining, based on the memory attribute information **[see Col. 3, Lines 40-43]**, a data transfer rate setting value as a rate of an upper limit value of a data transfer rate (maximum sustainable power) relative to a maximum data transfer rate **[see Col. 3, Lines 43-52 & Col. 4, Lines 32-45, "Maximum sustainable power represents upper limit value of the data transfer"]**, and for setting the determined data transfer rate setting value in the memory control device **[see Col. 5, Lines 1-4]**, the upper limit value of the data transfer rate being at which the memory control device accesses the memory module **[see Col. 3, Lines 43-52, "Maximum sustainable power"]**, and the maximum data transfer rate being at which the memory control device is able to access the memory module **[see Col. 4, Lines 46-49, "Maximum threshold bandwidth"]**.

IV. CLOSING COMMENTS

Conclusion

(a) **Status of Claims In the Application**

(i) Claims Rejected In the Application

Per the instant office action, claims 1-15 have received a first action on the merits and are subject of a first action non-final.

(b) **Directions of Future Correspondences**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Bertram whose telephone number is 571-270-1377. The examiner can normally be reached on Mon-Fri 8am-5pm ET (Alternate Fridays off).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RDB

DONALD SPARKS
SUPERVISORY PATENT EXAMINER